

ABSTRACT OF THE DISCLOSURE

5 The present invention provides a data processing apparatus and method for
controlling access to a memory unit. The data processing apparatus comprises a
processor operable in a plurality of modes and a plurality of domains, said plurality of
domains comprising a secure domain and a non-secure domain, said plurality of modes
including at least one non-secure mode being a mode in the non-secure domain and at
least one secure mode being a mode in the secure domain. The processor is operable
10 such that when executing a program in a secure mode the program has access to secure
data which is not accessible when the processor is operating in a non-secure mode. A
memory unit is also provided that comprises a plurality of entries and is operable to store
data required by the processor. Each entry is operable to store one or more data items
consisting of either secure data or non-secure data, and a flag is associated with each
15 entry in the memory unit to store a value indicating whether the one or more data items
stored in the associated entry are secure data or non-secure data. When the processor is
operating in the at least one non-secure mode, the memory unit is operable, upon receipt
of a memory access request issued by the processor when access to an item of data is
required, to prevent access to any data item within an entry of the memory unit that the
20 associated flag indicates has secure data stored therein.

(Figure 55)